

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of

Customer Number: 20277

Hideto HIDAKA

Confirmation Number: 7630

Serial No.: 10/644,750

Group Art Unit: 2818

Filed: August 21, 2003

Examiner: Not yet assigned

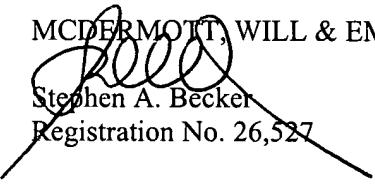
For: MIS SEMICONDUCTOR DEVICE HAVING IMPROVED GATE INSULATING FILM
RELIABILITYSUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

Mail Stop Issue Fee
 Commissioner for Patents
 P.O. Box 1450
 Alexandria, VA 22313-1450

Sir:

Further to the Information Disclosure Statement filed on August 21, 2003 in the captioned application, it is noted that one reference in the previously filed Information Disclosure Statement was inadvertently identified incorrectly on the corresponding PTO-1449 form. However, the correct reference was provided along with the IDS in the parent application Serial No. 09/813,796. Enclosed herewith is a revised PTO-1449 form which correctly identifies the reference in issue, as well as a marked-up copy of the original PTO-1449 form showing the error. It would be appreciated if the Examiner would initial the revised PTO-1449 form and return it to the Applicant and enter the revised PTO-1449 form into the file at the USPTO, so that all prior art references are properly identified on any patent issuing from this application.

Respectfully submitted,

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Date: March 17, 2004

INFORMATION DISCLOSURE
CITATION IN AN
APPLICATION

(PTO-1449)

ATTY. DOCKET NO.
57454-970SERIAL NO.
No. 10/644,750APPLICANT
Hideto HIDAKAFILING DATE
August 21, 2003GROUP
2818

U.S. PATENT DOCUMENTS

EXAMINER'S INITIALS	CITE NO.	Document Number Number-Kind Code ₂ (<i>if known</i>)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
	US	6,414,889	07/2002	Chen et al.	
	US	6,107,134	08/2000	Lu et al.	
	US	5,956,279	09/1999	Mo et al.	
	US	5,694,364	12/1997	Morishita et al.	
	US	5,379,260	01/1995	McClure	
	US				

FOREIGN PATENT DOCUMENTS

EXAMINER'S INITIALS	CITE NO.	Foreign Patent Document Country Codes-Number & Kind Codes (<i>if known</i>)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines Where Relevant Figures Appear	Translation	
						Yes	No

OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)

EXAMINER'S INITIALS	CITE NO.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published. `	
		"A Precise On-Chip Voltage Generator for a Gigascale DRAM with a Negative Word-Line Scheme", by Tanaka et al., IEEE Journal of Solid-State Circuits, Vol. 34, No. 8, 8/1999, pp. 1084-1090.	
		"Ultra LSI Memory" by Kiyoo Ito, Advanced Electronics Series, November 5, 1994, published by Baifukan, pp. 351-371.	
		"An Experimental 256-Mb DRAM with Boosted Sense-Ground Scheme", by Asakura et al., IEEE Journal of Solid-State Circuits, Vol. 29, No. 11, 11/1994, pp. 1303-1309.	

EXAMINER

DATE CONSIDERED

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

1 Applicant's unique citation designation number (optional). 2 Applicant is to place a check mark here if English language Translation is attached.

